What is claimed is:

1. A circuit board comprising:

first and second reference plane layers;

a first decoupling capacitor mounted to a surface of the first reference plane layer;

a second decoupling capacitor mounted to a surface of the second reference plane layer; and

vias extending generally along a direction through the first and second reference plane layers,

wherein the first and second decoupling capacitors are aligned generally along the direction to increase an amount of space in the circuit board through which the vias are extendable.

2. The circuit board of claim 1, wherein the vias comprise through-hole vias that extend from one side of the circuit to another side of the circuit board.

3. The circuit board of claim 1, further comprising additional first decoupling capacitors mounted to the surface of the first reference plane layer, and additional second decoupling capacitors mounted to the surface of the second reference plane layer,

wherein each pair of first and second decoupling capacitors are aligned generally along the direction such that multiple spaced-apart lines of decoupling capacitors are provided, each line of decoupling capacitors including a respective pair of first and second decoupling capacitors.

4. The circuit board of claim 3, wherein the vias extend through the circuit board in regions devoid of decoupling capacitors.

5. The circuit board of claim 4, further comprising a dielectric layer between the first and second reference plane layers, wherein the first and second decoupling capacitors are separated by at least the first and second reference plane layers and the dielectric layer, and the vias extend through the first and second reference plane layers and the dielectric layer.

6. The circuit board of claim 5, wherein each of the first decoupling capacitors includes a first electrode and a second electrode, the circuit board further comprising a first buried via electrically contacted to the first electrode of one of the first decoupling capacitors, the first buried via extending through the first reference plane layer and the dielectric layer to electrically contact the second reference plane layer.

7. The circuit board of claim 6, wherein each of the second decoupling capacitors includes first and second electrodes, the circuit board further comprising a second buried via electrically contacted to the first electrode of one of the second decoupling capacitors, the second buried via extending through the second reference plane layer and dielectric layer to electrically contact the first reference plane layer.

8. The circuit board of claim 7, further comprising layers provided above and below a core assembly including the first and second reference plane layers, dielectric layer, and first and second decoupling capacitors.

9. The circuit board of claim 3, wherein the first decoupling capacitors are spaced apart with respect to each other across the surface of the first reference plane layer, and the second decoupling capacitors are spaced apart with respect to each other across a surface of the second reference plane layer.

10. The circuit board of claim 9, further comprising:
first regions between the spaced apart first decoupling capacitors; and
second regions between the spaced apart second decoupling capacitors,
the first and second regions being generally aligned along the direction,
the vias extending through the circuit board through the first and second regions.

11. The circuit board of claim 3, further comprising:

a first core assembly including the first and second reference plane layers, a dielectric layer, and the first and second decoupling capacitors; and

a second core assembly including:

a third reference plane layer;

a fourth reference plane layer;

a second dielectric layer between the third and fourth reference plane layers;

third decoupling capacitors mounted to a surface of the third reference plane layers;

fourth decoupling capacitors mounted to a surface of the fourth reference plane layers;

wherein each pair of the third and fourth decoupling capacitors are aligned generally along the direction.

12. The circuit board of claim 11, wherein a group of first, second, third, and fourth decoupling capacitors are aligned along the direction.

13. A system comprising:

a power supply;

an integrated circuit device to be powered by the power supply; and

a circuit board on which the integrated circuit device is mounted, the circuit board comprising:

first and second reference plane layers;

first decoupling capacitors mounted to a surface of the first reference plane layer, the first decoupling capacitors being spaced apart across the surface of the first reference plane layer;

second decoupling capacitors mounted to a surface of the second reference plane layer, the second decoupling capacitors being spaced apart across the surface of the second reference plane layer; and

wherein each pair of the first and second decoupling capacitors are aligned generally along a direction that is generally perpendicular to a main surface of the circuit board to increase an amount of space in the circuit board for vias that are extendable through the first and second reference plane layers.

14. The system of claim 13, wherein the vias comprise through-hole vias that extend from one side of the circuit board to another side of the circuit board.

15. The system of claim 13, wherein the circuit board further comprises the vias, the vias extending through the circuit board in regions between spaced apart first and second decoupling capacitors.

16. The system of claim 15, wherein the circuit board further comprises a dielectric layer between the first and second reference plane layers, wherein each of the first decoupling capacitors includes a first electrode and a second electrode, and wherein the circuit board further comprises a first buried via electrically contacted to the first electrode of one of the decoupling capacitors, the first buried via extending through the first reference plane layer and the dielectric layer to electrically contact the second reference plane layer.

17. The system of claim 16, wherein each of the second decoupling capacitors includes first and second electrodes, wherein the circuit board further comprises a second buried via electrically contacted to the first electrode of one of the second decoupling capacitors, the second buried via extending through the second reference plane layer and dielectric layer to electrically contact the first reference plane layer.

18. The system of claim 17, wherein the circuit board further comprises layers provided above and below a core assembly including the first and second reference plane layers, dielectric layer, and first and second decoupling capacitors.

19. The system of claim 18, wherein the circuit board further comprises:
first regions between the spaced apart first decoupling capacitors; and
second regions between the spaced apart second decoupling capacitors,
the first and second regions being generally aligned along the direction,
the vias extending through the circuit board through the first and second regions.

20. A method, comprising:
providing first and second reference plane layers;
mounting a first decoupling capacitor to a surface of the first reference plane layer;
mounting a second decoupling capacitor to a surface of the second reference plane layer;
extending vias generally along a direction through the first and second reference plane layers; and
aligning the first and second decoupling capacitors generally along the direction to provide greater space to extend the vias.

21. The method of claim 20, wherein extending the vias comprises extending through-hole vias from a first main surface of the circuit board to another main surface of the circuit board.

22. The method of claim 20, further comprising:

mounting additional first decoupling capacitors to the surface of the first reference plane layer, and mounting additional second decoupling capacitors to the surface of the second reference plane layer; and

aligning each pair of first and second decoupling capacitors generally along the direction.

23. The method of claim 22, wherein extending the vias comprises extending the vias through the circuit board in regions between spaced apart first and second decoupling capacitors..

24. The method of claim 23, further comprising providing a dielectric layer between the first and second reference plane layers.

25. The method of claim 24, further comprising providing layers above and below a core assembly including the first and second reference plane layers, dielectric layer, and first and second decoupling capacitors.

26. The method of claim 22, further comprising:

providing first regions between spaced apart first decoupling capacitors; and

providing second regions between spaced apart second decoupling capacitors,

aligning the first and second regions along the direction,

wherein extending the vias comprises extending the vias through the circuit board through the first and second regions.